REMARKS

I. Formal Matters

Claims 1-7, 9 and 12-23 are currently pending in this application. Claims 8, 10 and 11 were previously cancelled. New claim 23 is presented via this Amendment. Applicant thanks the Examiner for withdrawing the prior objection to claim 1.

II. Claims

The Examiner objects to claim 22 due to a typographical error, which is hereby corrected. With respect to the alleged lack of antecedent basis with respect to the recitation of "said second capacitor dielectric film" appearing in the last line of claim 22, the Examiner's attention is directed to the penultimate paragraph of claim 22, which recites "...said step of forming said capacitor dielectric film comprises a step of forming a *first* capacitor dielectric film on said part of said interlayer film and a second capacitor dielectric film on said second HSG after removing said *first* HSG and said *first* polysilicon film..." Accordingly, Applicant respectfully requests withdrawal of the objections to claim 22.

Claims 1-7, 9 and 12-22 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Sung* in view of Applicant's Admitted Prior Art ("AAPA") and JP H11-284139 (hereinafter "*JP '139*"). Applicant respectfully traverses this rejection in view of the following remarks.

Independent Claims 1 and 16. Examiner relies on *JP '139* to allegedly provide the element of removing a *first* (*upper surface*) HSG and a *first* polysilicon layer, before forming the capacitor dielectric (OA page 4). *JP' 139* discloses the formation of a DRAM device, in contrast to Applicant's formation of a semiconductor device comprising CMOS logic and DRAM (claim 1 and 16). In applicant's amended claims, removal of upper surface (*first*) layers, before formation of capacitor dielectric, is performed on the CMOS side. Neither *Sung* nor *JP '139* disclose removing the *first* polysilicon layer (and removing the *first* HSG layer) from the *upper surface* on the CMOS side, before forming the capacitor dielectric. A proper §103(a) obviousness rejection will teach or suggest each and every element of the rejected claim. At least for failing to teach or suggest the element of removing the *first* polysilicon layer (and removing the *first* HSG layer) from the *upper surface* on the CMOS side, before forming the capacitor dielectric on the second HSG on the DRAM side, applicant asserts that the rejection of independent claims 1 and 16 under 35 U.S.C. §103(a) over *Sung* in view of *JP '139* should be withdrawn.

Withdrawal of the 35 U.S.C. §103(a) over *Sung* in view of *JP '139* rejection of dependent claims 2-7, 9, 12-15 and 17-21 (which incorporate all the novel and unobvious features of their respective independent claims) is also requested at least for depending from an allowable dependent claim.

New claim 23 is hereby added which recites a step of removing a *first* HSG and a *first* polysilicon film to expose a part of an interlayer film. Followed by a step of forming a dielectric

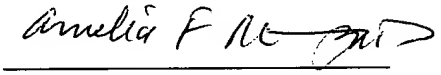
layer on the second HSG and on the exposed interlayer, where the second HSG is disposed in a groove, and wherein a groove forms inner capacitor walls.

In contrast, *Sung* does not form a capacitor dielectric film 38 upon the second HSG/polysilicon disposed in the inner walls of the capacitors and the exposed interlayer. *JP '139* teaches removing part 44A of the interlayer 44 disposed between grooves. Then *JP '139* teaches filling this space between capacitors with a dielectric film 56 and the upper electrode 58 (*JP '139* Figs. 6 -8; page 17, n-o). Thus, neither *Sung* nor *JP '139* teaches or suggests the above steps of new claim 23.

In view of the preceding amendments and remarks, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue that the Examiner feels may be best resolved through a personal or telephonic interview, the Examiner is kindly requested to contact the undersigned attorney at the local telephone number listed below.

A Petition for Extension of Time with appropriate fee accompanies this document. The USPTO is directed and authorized to charge all additional required fees (except the Issue/Publication Fees) to our Deposit Account No. 19-4880. Please also credit any over-payments to said Deposit Account.

Respectfully submitted,



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